

IRF540



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Product Preview

TMOS E-FET™ Power Field Effect Transistor

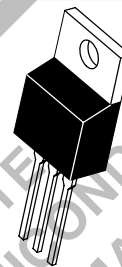
N-Channel Enhancement-Mode Silicon Gate

This advanced TMOS power FET is designed to withstand high energy in the avalanche and commutation modes. This new energy efficient design also offers a drain-to-source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters, and PWM motor controls. These devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical and offer additional safety margin against unexpected voltage transients.

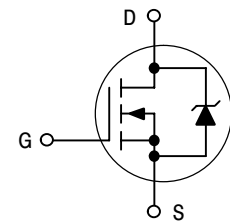
- Avalanche Energy Specified
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature

TMOS POWER FET
27 AMPERES, 100 VOLTS

$R_{DS(on)} = 0.070$ OHMS



CASE 221A-09
TO-220AB



MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|--|-----------------|------------|---------------------|
| Drain-to-Source Voltage | V_{DSS} | 100 | Vdc |
| Drain-to-Gate Voltage ($R_{GS} = 1.0\text{ M}\Omega$) | V_{DGR} | 100 | Vdc |
| Gate-to-Source Voltage — Continuous | V_{GS} | ± 20 | Vdc |
| — Non-repetitive ($t_p \leq 10\text{ ms}$) | V_{GSM} | ± 40 | Vpk |
| Drain Current — Continuous | I_D | 27 | Adc |
| — Continuous @ 100°C | I_D | 19 | |
| — Single Pulse ($t_p \leq 10\text{ }\mu\text{s}$) | I_{DM} | 95 | Apk |
| Total Power Dissipation | P_D | 145 | Watts |
| Derate above 25°C | | 1.16 | W/ $^\circ\text{C}$ |
| Operating and Storage Temperature Range | T_J, T_{stg} | -55 to 150 | $^\circ\text{C}$ |
| Single Pulse Drain-to-Source Avalanche Energy — STARTING $T_J = 25^\circ\text{C}$ ($V_{DD} = 50\text{ Vdc}$, $V_{GS} = 10\text{ Vdc}$, PEAK $I_L = 27\text{ Apk}$, $L = 1.0\text{ mH}$, $R_G = 25\text{ }\Omega$) | E_{AS} | 365 | mJ |
| Thermal Resistance — Junction-to-Case | $R_{\theta JC}$ | 0.86 | $^\circ\text{C/W}$ |
| — Junction-to-Ambient | $R_{\theta JA}$ | 62.5 | |
| Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds | T_L | 260 | $^\circ\text{C}$ |

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

E-FET is a trademark of Motorola, Inc. TMOS is a registered trademark of Motorola, Inc.

IRF540

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|----------------------|-----|----------|-----------|--------------|
| OFF CHARACTERISTICS | | | | | |
| Drain-to-Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 0.25 mAdc) Temperature Coefficient (Positive) | V _{(BR)DSS} | 100 | — 116 | — | Vdc mV/°C |
| Zero Gate Voltage Drain Current (V _{DS} = 100 Vdc, V _{GS} = 0 Vdc) (V _{DS} = 100 Vdc, V _{GS} = 0 Vdc, T _J = 125°C) | I _{DSS} | — | — | 10 100 | μAdc |
| Gate-Body Leakage Current (V _{GS} = ±20 Vdc, V _{DS} = 0 Vdc) | I _{GSS} | — | — | 100 | nAdc |

ON CHARACTERISTICS⁽¹⁾

| | | | | | | |
|--|--------------------------|---------------------|-----|------------|------------|--------------|
| Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 250 μAdc) Threshold Temperature Coefficient (Negative) | Cpk ≥ 2.0 ⁽³⁾ | V _{GS(th)} | 2.0 | 2.9 6.8 | 4.0 | Vdc mV/°C |
| Static Drain-to-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 15 Adc) | Cpk ≥ 2.0 ⁽³⁾ | R _{DS(on)} | — | 0.047 | 0.070 | Ohms |
| Drain-to-Source On-Voltage (V _{GS} = 10 Vdc, I _D = 27 Adc) (V _{GS} = 10 Vdc, I _D = 15 Adc, T _J = 125°C) | | V _{DS(on)} | — | — | 1.9 1.8 | Vdc |
| Forward Transconductance (V _{DS} = 15 Vdc, I _D = 15 Adc) | | g _{FS} | 6.0 | 15 | — | Mhos |

DYNAMIC CHARACTERISTICS

| | | | | | | |
|----------------------|---|------------------|---|------|------|----|
| Input Capacitance | (V _{DS} = 25 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz) | C _{iss} | — | 1460 | 1600 | pF |
| Output Capacitance | | C _{oss} | — | 390 | 800 | |
| Transfer Capacitance | | C _{rss} | — | 120 | 300 | |

SWITCHING CHARACTERISTICS⁽²⁾

| | | | | | | |
|-------------------------------|--|---------------------|---|------|----|----|
| Turn-On Delay Time | (V _{DD} = 30 Vdc, I _D = 15 Adc, V _{GS} = 10 Vdc, R _G = 4.7 Ω) | t _{d(on)} | — | 11.6 | 30 | ns |
| Rise Time | | t _r | — | 50 | 60 | |
| Turn-Off Delay Time | | t _{d(off)} | — | 26 | 80 | |
| Fall Time | | t _f | — | 19 | 30 | |
| Gate Charge (See Figure 8) | (V _{DS} = 80 Vdc, I _D = 27 Adc, V _{GS} = 10 Vdc) | Q _T | — | 50 | 60 | nC |
| | | Q ₁ | — | 9.0 | — | |
| | | Q ₂ | — | 26 | — | |
| | | Q ₃ | — | 20 | — | |

SOURCE-DRAIN DIODE CHARACTERISTICS

| | | | | | | |
|--|-----------------|---|--------------|-----|---|-----|
| Forward On-Voltage (I _S = 27 Adc, V _{GS} = 0 Vdc) (I _S = 27 Adc, V _{GS} = 0 Vdc, T _J = 125°C) | V _{SD} | — | 0.93 0.84 | 2.4 | — | Vdc |
| Reverse Recovery Time | t _{rr} | — | 110 | — | — | ns |
| | t _a | — | 100 | — | — | |
| | t _b | — | 10 | — | — | |
| Reverse Recovery Stored Charge | Q _{RR} | — | 0.67 | — | — | μC |

INTERNAL PACKAGE INDUCTANCE

| | | | | | | |
|--|----------------|---|------------|---|---|----|
| Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die) | L _d | — | 3.5 4.5 | — | — | nH |
| Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad) | L _s | — | 7.5 | — | — | |

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

(3) Reflects typical values. $Cpk = \frac{|\text{Max limit} - \text{Typ}|}{3 \times \text{sigma}}$

TYPICAL ELECTRICAL CHARACTERISTICS

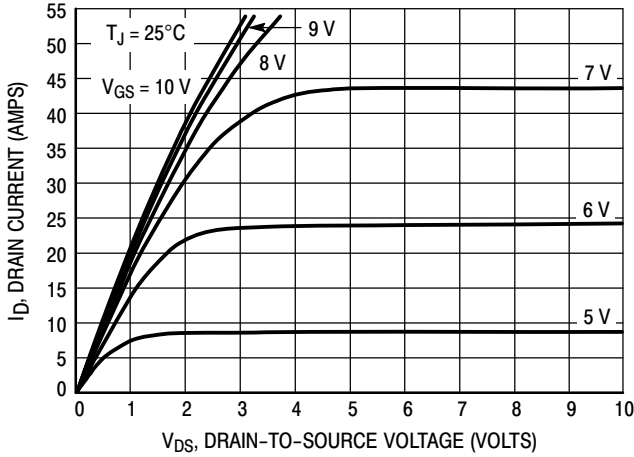


Figure 1. On-Region Characteristics

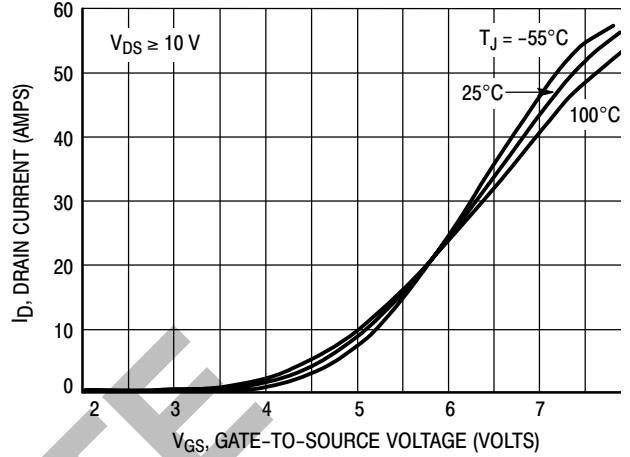


Figure 2. Transfer Characteristics

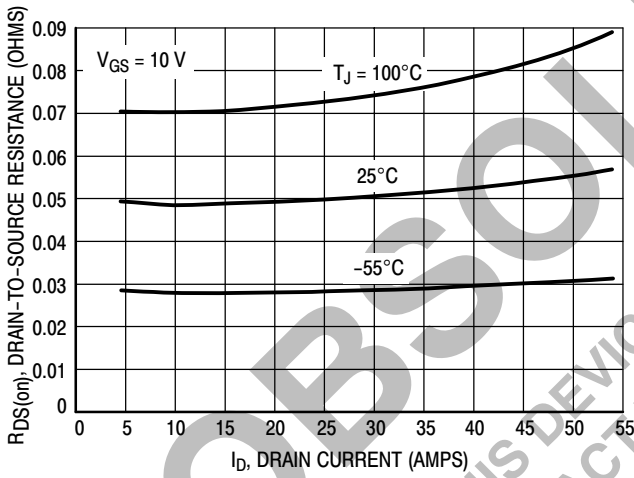


Figure 3. On-Resistance versus Drain Current and Temperature

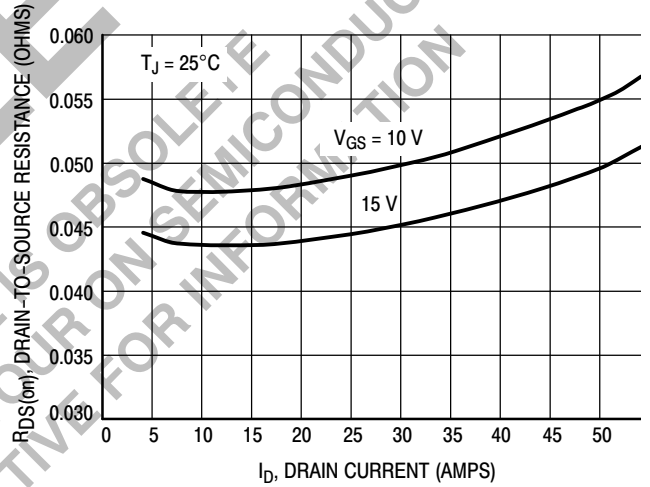


Figure 4. On-Resistance versus Drain Current and Gate Voltage

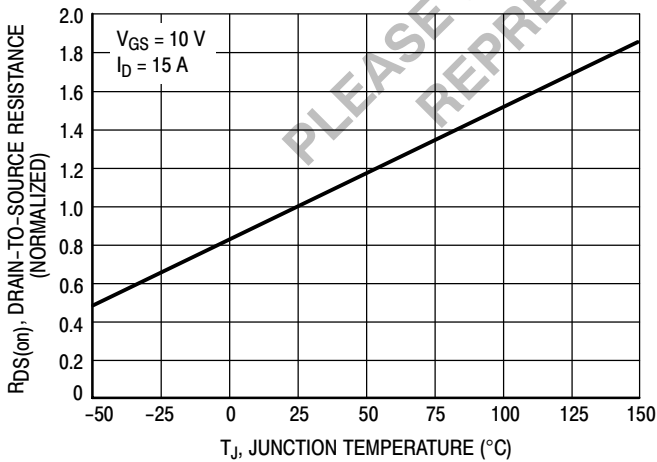


Figure 5. On-Resistance Variation with Temperature

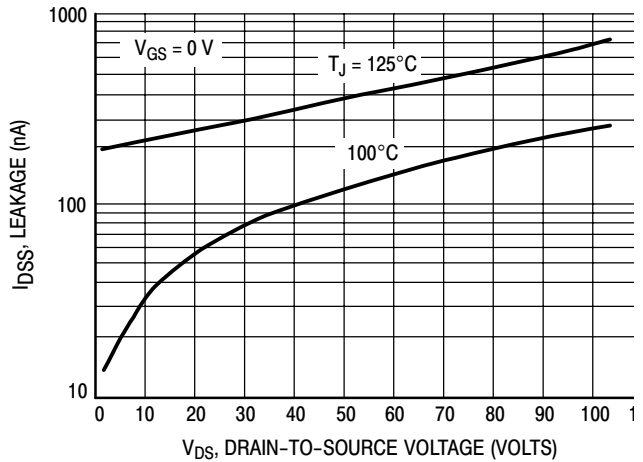


Figure 6. Drain-to-Source Leakage Current versus Voltage

TYPICAL ELECTRICAL CHARACTERISTICS

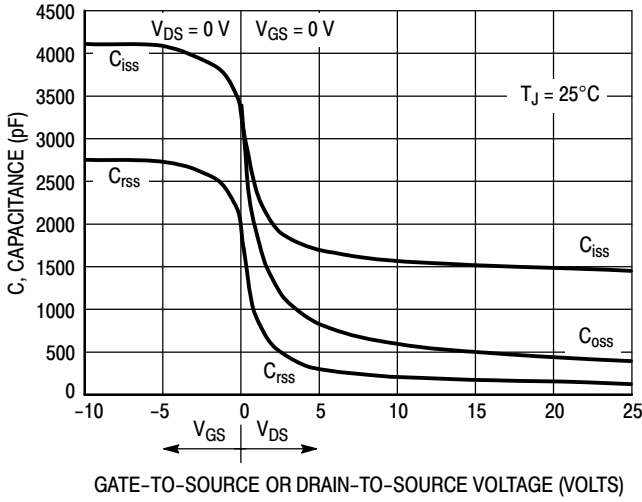


Figure 7. Capacitance Variation

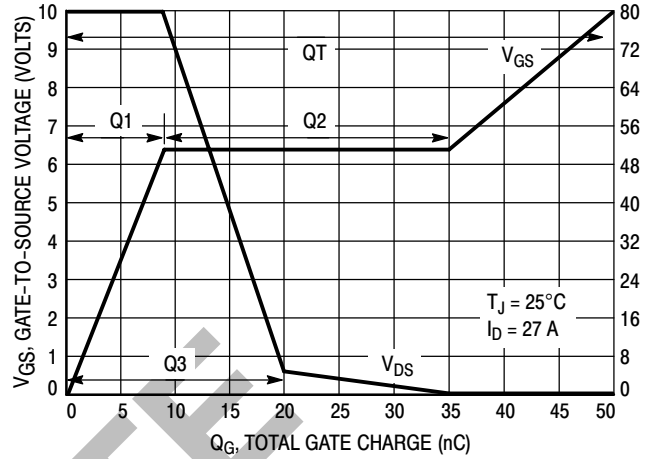


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

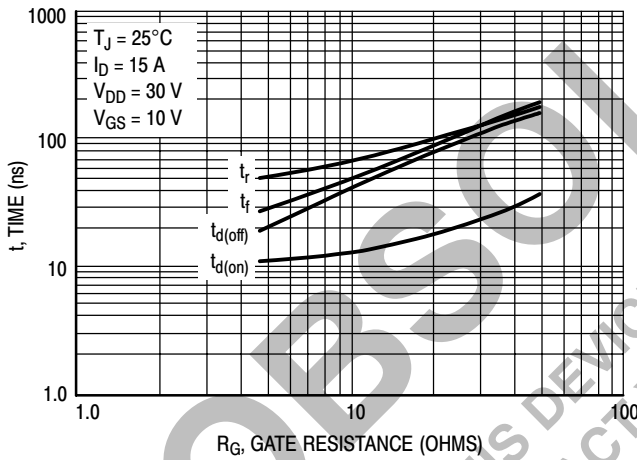


Figure 9. Resistive Switching Time Variation versus Gate Resistance

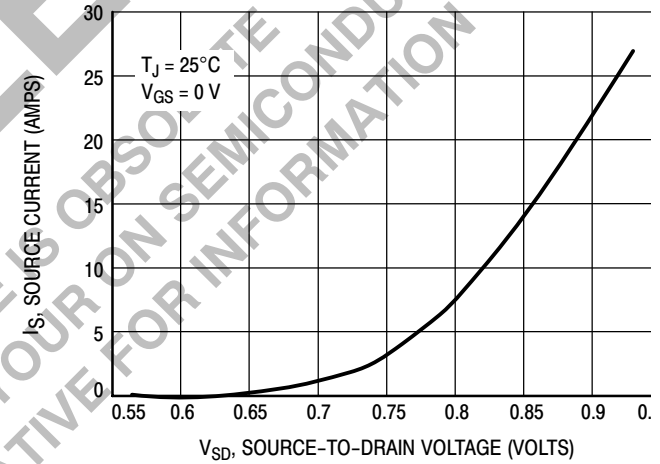


Figure 10. Diode Forward Voltage versus Current

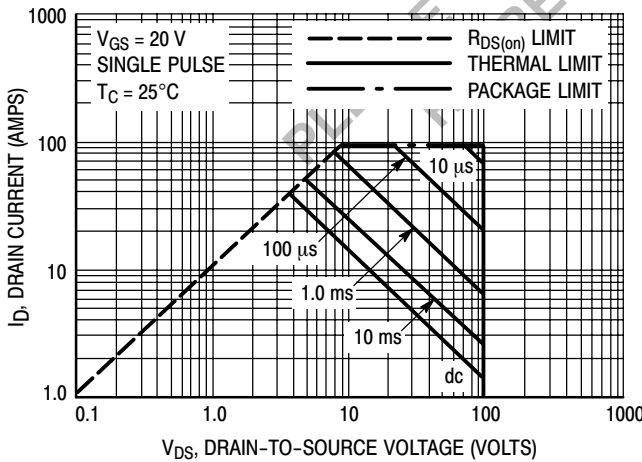


Figure 11. Maximum Rated Forward Biased Safe Operating Area

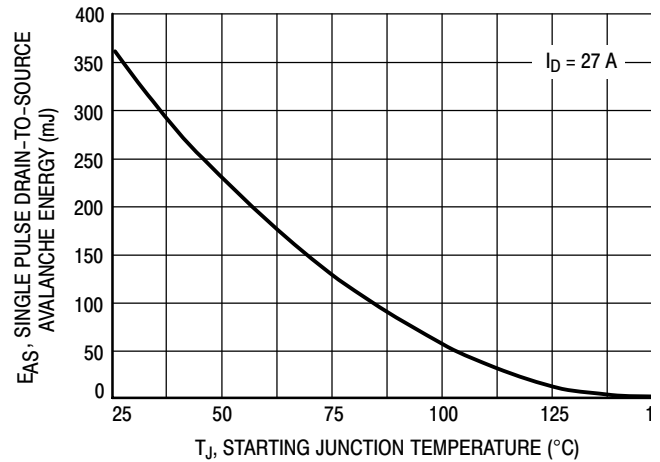


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

IRF540

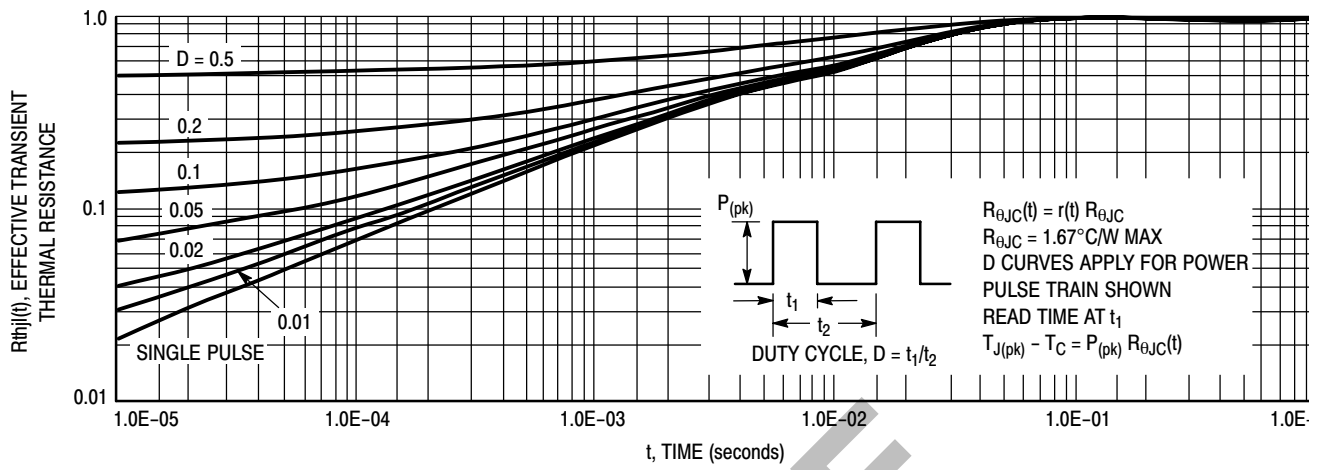


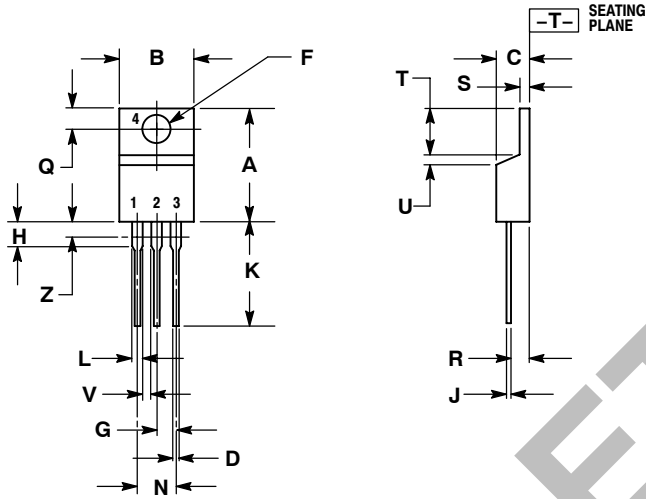
Figure 13. Thermal Response

OBSOLETE
 THIS DEVICE IS OBSOLETE
 PLEASE CONTACT YOUR ON SEMICONDUCTOR
 REPRESENTATIVE FOR INFORMATION

IRF540

PACKAGE DIMENSIONS

CASE 221A-09 (TO-220AB) ISSUE Z



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

| DIM | INCHES | | MILLIMETERS | |
|-----|--------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.570 | 0.620 | 14.48 | 15.75 |
| B | 0.380 | 0.405 | 9.66 | 10.28 |
| C | 0.160 | 0.190 | 4.07 | 4.82 |
| D | 0.025 | 0.035 | 0.64 | 0.88 |
| F | 0.142 | 0.147 | 3.61 | 3.73 |
| G | 0.095 | 0.105 | 2.42 | 2.66 |
| H | 0.110 | 0.155 | 2.80 | 3.93 |
| J | 0.018 | 0.025 | 0.46 | 0.64 |
| K | 0.500 | 0.562 | 12.70 | 14.27 |
| L | 0.045 | 0.060 | 1.15 | 1.52 |
| N | 0.190 | 0.210 | 4.83 | 5.33 |
| Q | 0.100 | 0.120 | 2.54 | 3.04 |
| R | 0.080 | 0.110 | 2.04 | 2.79 |
| S | 0.045 | 0.055 | 1.15 | 1.39 |
| T | 0.235 | 0.255 | 5.97 | 6.47 |
| U | 0.000 | 0.050 | 0.00 | 1.27 |
| V | 0.045 | --- | 1.15 | --- |
| Z | --- | 0.080 | --- | 2.04 |

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